Fast, Precision Comparator

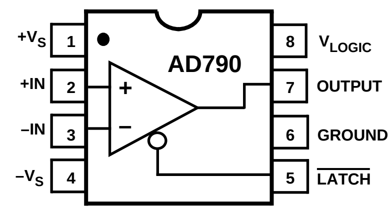
AD790

FEATURES
45 ns max Propagation Delay
Single +5 V or Dual ±15 V Supply Operation
CMOS or TTL Compatible Output
250 μV max Input Offset Voltage
500 μV max Input Hysteresis Voltage
15 V max Differential Input Voltage
Onboard Latch
60 mW Power Dissipation
Available in 8-Pin Plastic and Hermetic Cerdip Packages
MIL-STD-883B Processing Available
Available in Tape and Reel in Accordance with EIA-481A Standard

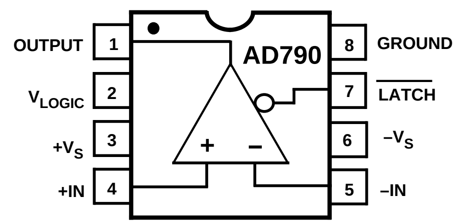
APPLICATIONS
Zero-Crossing Detectors
Overvoltage Detectors
Pulse-Width Modulators
Precision Rectifiers
Discrete A/D Converters
Delta-Sigma Modulator A/Ds

CONNECTION DIAGRAMS

8-Pin Plastic Mini-DIP (N) and Cerdip (Q) Packages



8-Pin SOIC (R) Package



PRODUCT DESCRIPTION

The AD790 is a fast (45 ns), precise voltage comparator, with a number of features that make it exceptionally versatile and easy to use. The AD790 may operate from either a single +5 V supply or a dual ±15 V supply. In the single-supply mode, the AD790's inputs may be referred to ground, a feature not found in other comparators. In the dual-supply mode it has the unique ability of handling a maximum differential voltage of 15 V across its input terminals, easing their interfacing to large amplitude and dynamic signals.

This device is fabricated using Analog Devices' Complementary Bipolar (CB) process–which gives the AD790's combination of fast response time and outstanding input voltage resolution (1 mV max). To preserve its speed and accuracy, the AD790 incorporates a "low glitch" output stage that does not exhibit the large current spikes normally found in TTL or CMOS output stages. Its controlled switching reduces power supply disturbances that can feed back to the input and cause undesired oscillations. The AD790 also has a latching function which makes it suitable for applications requiring synchronous operation.

The AD790 is available in five performance grades. The AD790J and the AD790K are rated over the commercial temperature range of 0°C to +70°C. The AD790A and AD790B are rated over the industrial temperature range of –40°C to +85°C. The AD790S is rated over the military temperature range of –55°C to +125°C and is available processed to MIL-STD-883B, Rev. C.

PRODUCT HIGHLIGHTS

1. The AD790's combination of speed, precision, versatility and low cost makes it suitable as a general purpose comparator in analog signal processing and data acquisition systems.
2. Built-in hysteresis and a low-glitch output stage minimize the chance of unwanted oscillations, making the AD790 easier to use than standard open-loop comparators.
3. The hysteresis combined with a wide input voltage range enables the AD790 to respond to both slow, low level (e.g., 10 mV) signals and fast, large amplitude (e.g., 10 V) signals.
4. A wide variety of supply voltages are acceptable for operation of the AD790, ranging from single +5 V to dual +5 V/–12 V, ±5 V, or +5 V/±15 V supplies.
5. The AD790's power dissipation is the lowest of any comparator in its speed range.
6. The AD790's output swing is symmetric between V_{LOGIC} and ground, thus providing a predictable output under a wide range of input and output conditions.

REV. B

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AD790–SPECIFICATIONS

DUAL SUPPLY (Operation @ +25°C and $+V_S$ = +15 V, $-V_S$ = –15 V, V_{LOGIC} = +5 V unless otherwise noted)

Parameter	Conditions	AD790J/A Min	AD790J/A Typ	AD790J/A Max	AD790K/B Min	AD790K/B Typ	AD790K/B Max	AD790S Min	AD790S Typ	AD790S Max	Units
RESPONSE CHARACTERISTIC	100 mV Step										
Propagation Delay, t_{PD}	5 mV Overdrive		40	45		40	45		40	45	ns
	T_{MIN} to T_{MAX}			45/50			45/50			60	ns
OUTPUT CHARACTERISTICS											
Output HIGH Voltage, V_{OH}	1.6 mA Source		4.65			4.65			4.65		
	6.4 mA Source	**4.3**	4.45		**4.3**	4.45		**4.3**	4.45		V
	T_{MIN} to T_{MAX}	4.3/**4.3**			**4.3**			**4.3**			V
Output LOW Voltage, V_{OL}	1.6 mA Sink		0.35			0.35			0.35		V
	6.4 mA Sink		0.44	**0.5**		0.44	**0.5**		0.44	**0.5**	V
	T_{MIN} to T_{MAX}			0.5/**0.5**			**0.5**			**0.5**	V
INPUT CHARACTERISTICS											
Offset Voltage[1]			0.2	**1.0**		0.05	**0.25**		0.2	**1.0**	mV
	T_{MIN} to T_{MAX}			1.5			**0.5**			**1.5**	mV
Hysteresis[2]	T_{MIN} to T_{MAX}	0.3	0.4	0.6	**0.3**	0.4	**0.5**	**0.3**	0.4	**0.65**	mV
Bias Current	Either Input		2.5	5		1.8	**3.5**		2.5	**5**	µA
	T_{MIN} to T_{MAX}			6.5			**4.5**			**7**	µA
Offset Current			0.04	**0.25**		0.02	**0.15**		0.04	**0.25**	µA
	T_{MIN} to T_{MAX}			0.3			**0.2**			**0.4**	µA
Power Supply											
Rejection Ratio DC	V_S ±20%	**80**	90		**88**	100		**80**	90		dB
	T_{MIN} to T_{MAX}	76	88		**85**	93		**76**	85		dB
Input Voltage Range											
Differential Voltage	V_S ≤±15 V			**±V_S**			**±V_S**			**±V_S**	V
Common Mode		$-V_S$		$+V_S$–2 V	$-V_S$		$+V_S$–2 V	$-V_S$		$+V_S$–2 V	V
Common Mode											
Rejection Ratio	–10 V<V_{CM} <+10 V	**80**	95		**88**	105		**80**	95		dB
	T_{MIN} to T_{MAX}	76	90		**85**	100		**76**	88		dB
Input Impedance			20‖2			20‖2			20‖2		MΩ‖pF
LATCH CHARACTERISTICS											
Latch Hold Time, t_H			25	35		25	35		25	35	ns
Latch Setup Time, t_S			5	10		5	10		5	10	ns
LOW Input Level, V_{IL}	T_{MIN} to T_{MAX}			0.8			**0.8**			**0.8**	V
HIGH Input Level, V_{IH}	T_{MIN} to T_{MAX}	1.6			**1.6**			**1.6**			V
Latch Input Current			2.3	5		2.3	**3.5**		2.3	**5**	µA
	T_{MIN} to T_{MAX}			7			**5**			**8**	µA
SUPPLY CHARACTERISTICS											
Diff Supply Voltage[3]	V_{LOGIC} = 5 V										
	T_{MIN} to T_{MAX}	4.5		33	**4.5**		**33**	**4.7**		**33**	V
Logic Supply	T_{MIN} to T_{MAX}	4.0		7	**4.0**		**7**	**4.2**		**7**	V
Quiescent Current											
$+V_S$	$+V_S$ = 15 V		8	**10**		8	**10**		8	**10**	mA
$-V_S$	$-V_S$ = –15 V		4	**5**		4	**5**		4	**5**	mA
V_{LOGIC}	V_{LOGIC} = 5 V		2	**3.3**		2	**3.3**		2	**3.3**	mA
Power Dissipation				**242**			**242**			**242**	mW
TEMPERATURE RANGE											
Rated Performance	T_{MIN} to T_{MAX}	0 to +70/–40 to +85			0 to +70/–40 to +85				–55 to +125		°C

NOTES

[1]Defined as the average of the input voltages at the low to high and high to low transition points. Refer to Figure 14.

[2]Defined as half the magnitude between the input voltages at the low to high and high to low transition points. Refer to Figure 14.

[3]$+V_S$ must be no lower than (V_{LOGIC} –0.5 V) in any supply operating conditions, except during power up.

All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units at final test.

Specifications subject to change without notice.

SINGLE SUPPLY (Operation @ +25°C and $+V_S = V_{LOGIC} = +5$ V, $-V_S = 0$ V unless otherwise noted)[1]

Parameter	Conditions	AD790J/A Min	Typ	Max	AD790K/B Min	Typ	Max	AD790S Min	Typ	Max	Units
RESPONSE CHARACTERISTIC	100 mV Step										
Propagation Delay, t_{PD}	5 mV Overdrive		45	50		45	50		45	50	ns
	T_{MIN} to T_{MAX}			50/60			50/60			65	ns
OUTPUT CHARACTERISTICS											
Output HIGH Voltage, V_{OH}	1.6 mA Source		4.65			4.65			4.65		
	6.4 mA Source	**4.3**	4.45		**4.3**	4.45		**4.3**	4.45		V
	T_{MIN} to T_{MAX}	4.3			**4.3**			**4.3**			V
Output LOW Voltage, V_{OL}	1.6 mA Sink		0.35			0.35			0.35		V
	6.4 mA Sink		0.44	**0.5**		0.44	**0.5**		0.44	**0.5**	V
	T_{MIN} to T_{MAX}			0.5			**0.5**			**0.5**	V
INPUT CHARACTERISTICS											
Offset Voltage[2]			0.45	**1.5**		0.35	**0.6**		0.45	**1.5**	mV
	T_{MIN} to T_{MAX}			2.0			**0.85**			**2.0**	mV
Hysteresis[3]	T_{MIN} to T_{MAX}	0.3	0.5	0.75	**0.3**	0.5	**0.65**	**0.3**	0.7	**1.0**	mV
Bias Current	Either Input		2.7	5		2.0	**3.5**		2.7	**5**	µA
	T_{MIN} to T_{MAX}			7			**5**			**8**	µA
Offset Current			0.04	**0.25**		0.02	**0.15**		0.04	**0.25**	µA
	T_{MIN} to T_{MAX}			0.3			**0.2**			**0.4**	µA
Power Supply											
Rejection Ratio DC	$4.5 \text{ V} \leq V_S \leq 5.5 \text{ V}$	**80**	90		**86**	100		**80**	90		dB
	T_{MIN} to T_{MAX}	76/**76**	88		**82**	93		**76**	85		dB
Input Voltage Range											
Differential Voltage				**±V_S**			**±V_S**			**±V_S**	V
Common Mode		0		$+V_S$–2 V	0		$+V_S$–2 V	0		$+V_S$–2 V	V
Input Impedance			20‖2			20‖2			20‖2		MΩ‖pF
LATCH CHARACTERISTICS											
Latch Hold Time, t_H			25	35		25	35		25	35	ns
Latch Setup Time, t_S			5	10		5	10		5	10	ns
LOW Input Level, V_{IL}	T_{MIN} to T_{MAX}			0.8			**0.8**			**0.8**	V
HIGH Input Level, V_{IH}	T_{MIN} to T_{MAX}	1.6			**1.6**			**1.6**			V
Latch Input Current			2.3	**5**		2.3	**3.5**		2.3	**5**	µA
	T_{MIN} to T_{MAX}			7			**5**			**8**	µA
SUPPLY CHARACTERISTICS											
Supply Voltage[4]	T_{MIN} to T_{MAX}	4.5		7	**4.5**		**7**	**4.7**		**7**	V
Quiescent Current			10	**12**		10	**12**		10	**12**	mA
Power Dissipation				**60**			**60**			**60**	mW
TEMPERATURE RANGE											
Rated Performance	T_{MIN} to T_{MAX}	0 to +70/–40 to +85			0 to +70/–40 to +85				–55 to +125		°C

NOTES
[1] Pin 1 tied to Pin 8, and Pin 4 tied to Pin 6.
[2] Defined as the average of the input voltages at the low to high and high to low transition points. Refer to Figure 14.
[3] Defined as half the magnitude between the input voltages at the low to high and high to low transition points. Refer to Figure 14.
[4] $-V_S$ must not be connected above ground.

All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units at final test.
Specifications subject to change without notice.

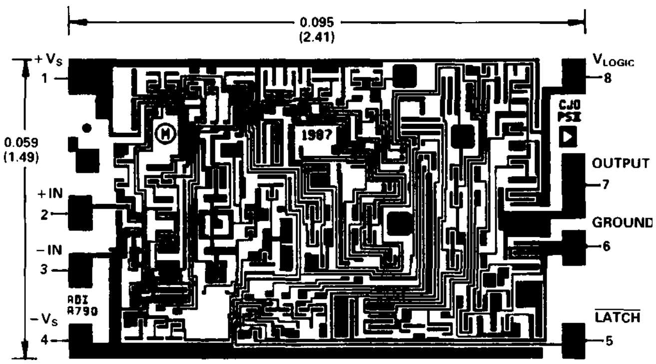
ABSOLUTE MAXIMUM RATINGS[1, 2]

Supply Voltage . . . . ±18 V
Internal Power Dissipation[2] . . . . 500 mW
Differential Input Voltage . . . . ±16.5 V
Output Short Circuit Duration . . . . Indefinite
Storage Temperature Range
  (N, R) . . . . –65°C to +125°C
  (Q) . . . . –65°C to +150°C
Lead Temperature Range (Soldering 60 sec) . . . . +300°C
Logic Supply Voltage . . . . 7 V

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Thermal characteristics: plastic N-8 package: θ_{JA} = 90°C/watt; ceramic Q-8 package: θ_{JA} = 110°C/watt, θ_{JC} = 30°C/watt. SOIC (R-8) package: θ_{JA} = 160°C watt; θ_{JC} = 42°C/watt.

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).
Call factory for chip specifications.



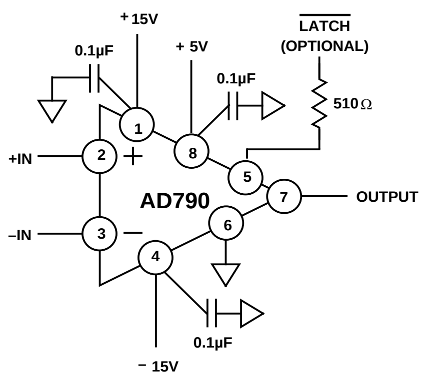


Figure 1. Basic Dual Supply Configuration (N, Q Package Pinout)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD790JN	0°C to +70°C	Plastic DIP	N-8
AD790JR	0°C to +70°C	SOIC	SO-8
AD790JR-REEL	0°C to +70°C	Reel	
AD790JR-REEL7	0°C to +70°C	SOIC	R-8
AD790KN	0°C to +70°C	Plastic DIP	N-8
AD790AQ	–40°C to +85°C	Cerdip	Q-8
AD790BQ	–40°C to +85°C	Cerdip	Q-8
AD790SQ	–55°C to +125°C	Cerdip	Q-8
AD790SQ/883B	–55°C to +125°C	Cerdip	Q-8
AD790S Chips	–55°C to +125°C	Die	

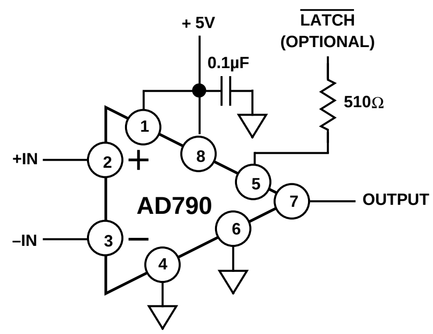


Figure 2. Basic Single Supply Configuration (N, Q Package Pinout)

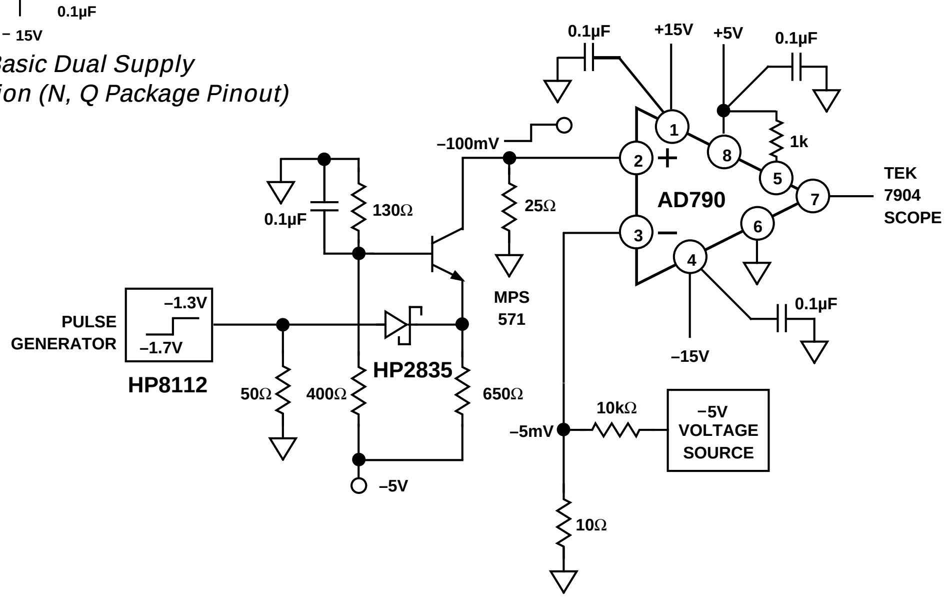


Figure 3. Response Time Test Circuit (N, Q Package Pinout)

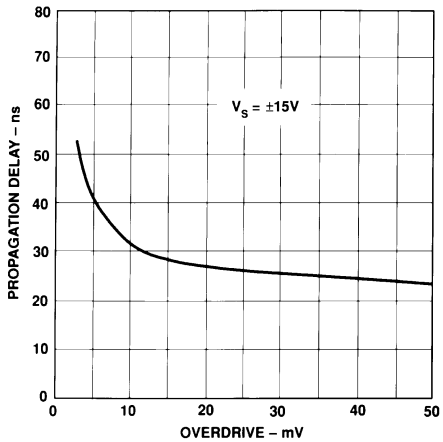


Figure 4. Propagation Delay vs. Overdrive

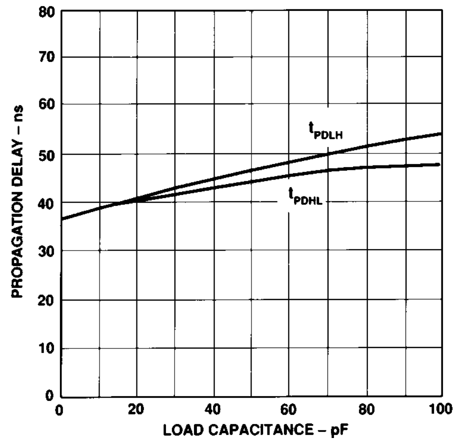


Figure 5. Propagation Delay vs. Load Capacitance

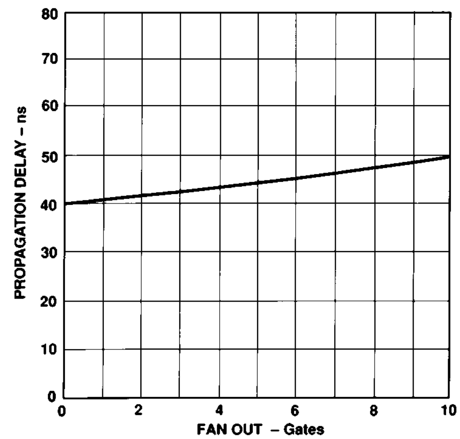


Figure 6. Propagation Delay vs. Fanout (LSTTL and CMOS)

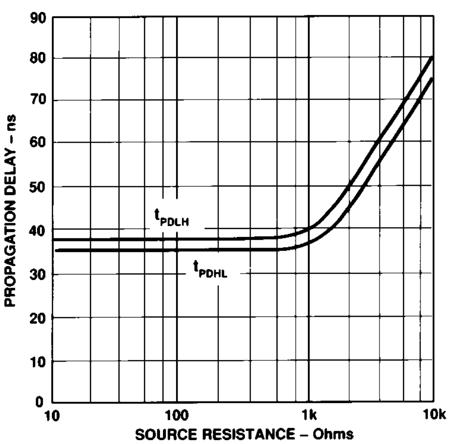


Figure 7. Propagation Delay vs. Source Resistance

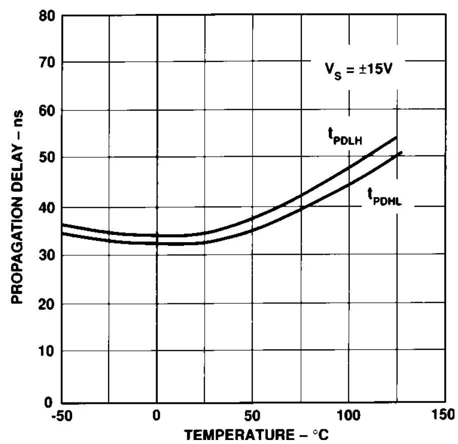


Figure 8. Propagation Delay vs. Temperature

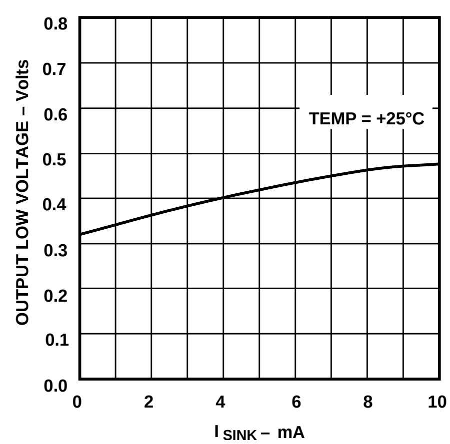


Figure 9. Output Low Voltage vs. Sink Current

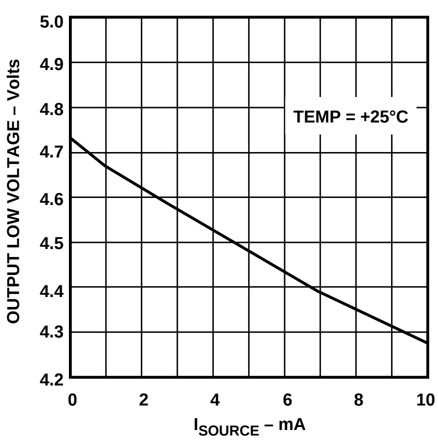


Figure 10. Output High Voltage vs. Source Current

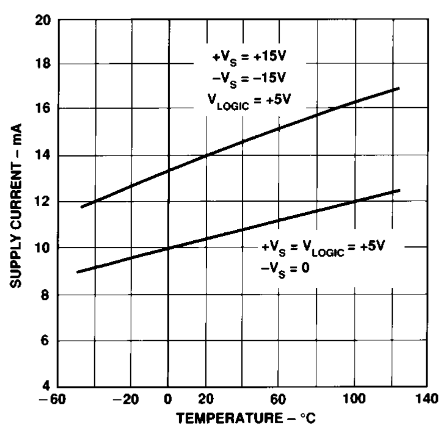


Figure 11. Total Supply Current vs. Temperature

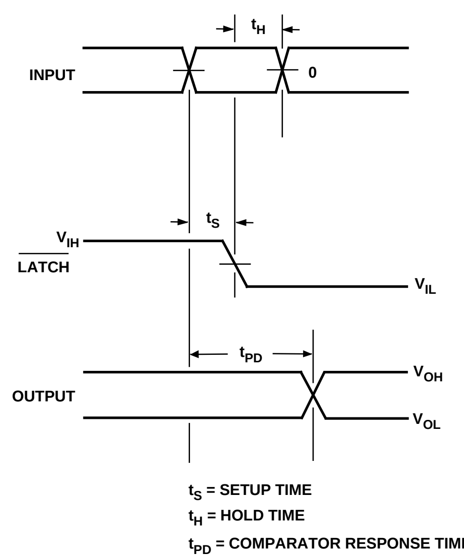


Figure 12. Latch Timing

CIRCUIT DESCRIPTION

The AD790 possesses the overall characteristics of a standard monolithic comparator: differential inputs, high gain and a logic output. However, its function is implemented with an architecture which offers several advantages over previous comparator designs. Specifically, the output stage alleviates some of the limitations of classic "TTL" comparators and provides a symmetric output. A simplified representation of the AD790 circuitry is shown in Figure 13.

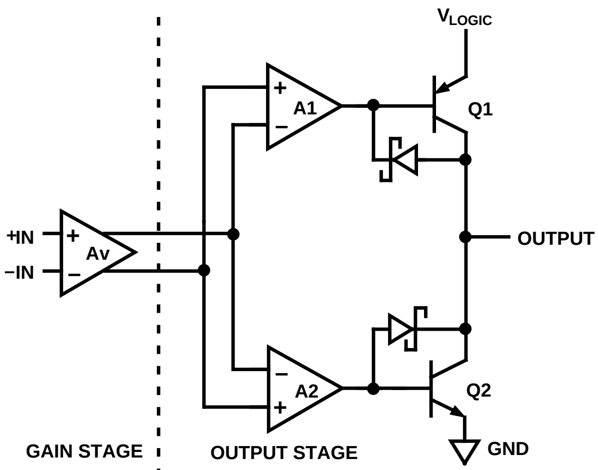


Figure 13. AD790 Block Diagram

The output stage takes the amplified differential input signal and converts it to a single-ended logic output. The output swing is defined by the pull-up PNP and the pull-down NPN. These produce inherent rail-to-rail output levels, compatible with CMOS logic, as well as TTL, without the need for clamping to internal bias levels. Furthermore, the pull-up and pull-down levels are symmetric about the center of the supply range and are referenced off the V_{LOGIC} supply and ground. The output stage has nearly symmetric dynamic drive capability, yielding equal rise and fall times into subsequent logic gates.

Unlike classic TTL or CMOS output stages, the AD790 circuit does not exhibit large current spikes due to unwanted current flow between the output transistors. The AD790 output stage has a controlled switching scheme in which amplifiers A1 and A2 drive the output transistors in a manner designed to reduce the current flow between Q1 and Q2. This also helps minimize the disturbances feeding back to the input which can cause troublesome oscillations.

The output high and low levels are well controlled values defined by V_{LOGIC} (+5 V), ground and the transistor equivalent "Schottky" clamps and are compatible with TTL and CMOS logic requirements. The fanout of the output stage is shown in Figure 6 for standard LSTTL or HCMOS gates. Output drive behavior vs. capacitive load is shown in Figure 5.

HYSTERESIS

The AD790 uses internal feedback to develop hysteresis about the input reference voltage. Figure 14 shows how the input offset voltage and hysteresis terms are defined. Input offset voltage (V_{OS}) is the difference between the center of the hysteresis range and the ground level. This can be either positive or negative. The hysteresis voltage (V_H) is one-half the width of the hysteresis range. This built-in hysteresis allows the AD790 to avoid oscillation when an input signal slowly crosses the ground level.

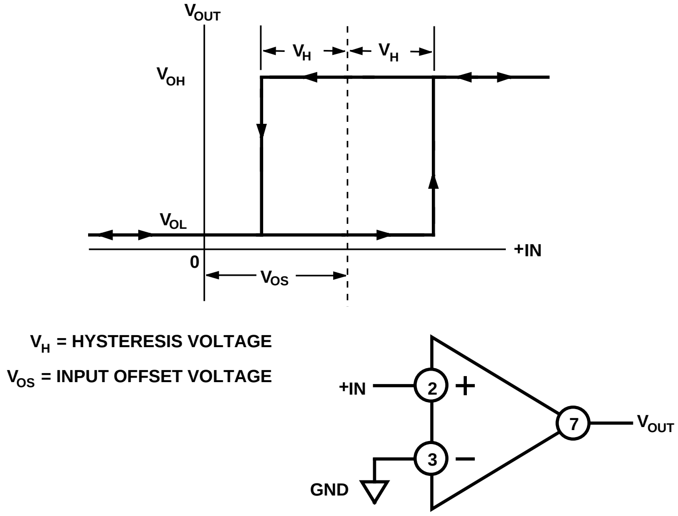


Figure 14. Hysteresis Definitions (N, Q Package Pinout)

SUPPLY VOLTAGE CONNECTIONS

The AD790 may be operated from either single or dual supply voltages. Internally, the V_{LOGIC} circuitry and the analog front-end of the AD790 are connected to separate supply pins. If dual supplies are used, any combination of voltages in which $+V_S \geq V_{LOGIC} - 0.5$ V and $-V_S \leq 0$ may be chosen. For single supply operation (i.e., $+V_S = V_{LOGIC}$), the supply voltage can be operated between 4.5 V and 7 V. Figure 15 shows some other examples of typical supply connections possible with the AD790.

BYPASSING AND GROUNDING

Although the AD790 is designed to be stable and free from oscillations, it is important to properly bypass and ground the power supplies. Ceramic 0.1 µF capacitors are recommended and should be connected directly at the AD790's supply pins. These capacitors provide transient currents to the device during comparator switching. The AD790 has three supply voltage pins, $+V_S$, $–V_S$ and V_{LOGIC}. It is important to have a common ground lead on the board for the supply grounds and the GND pin of the AD790 to provide the proper return path for the supply current.

LATCH OPERATION

The AD790 has a latch function for retaining input information at the output. The comparator decision is "latched" and the output state is held when Pin 5 is brought low. As long as Pin 5 is kept low, the output remains in the high or low state, and does not respond to changing inputs. Proper capture of the input signal requires that the timing relationships shown in Figure 12 are followed. Pin 5 should be driven with CMOS or TTL logic levels.

The output of the AD790 will respond to the input when Pin 5 is at a high logic level. When not in use, Pin 5 should be connected to the positive logic supply. When using dual supplies, it is recommended that a 510 Ω resistor be placed in series with Pin 5 and the driving logic gate to limit input currents during power up.

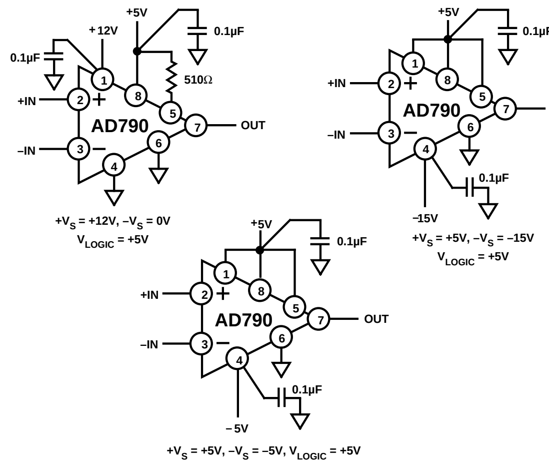


Figure 15. Typical Power Supply Connections (N, Q Package Pinout)

Window Comparator for Overvoltage Detection

The wide differential input range of the AD790 makes it suitable for monitoring large amplitude signals. The simple overvoltage detection circuit shown in Figure 16 illustrates direct connection of the input signal to the high impedance inputs of the comparator without the need for special clamp diodes to limit the differential input voltage across the inputs.

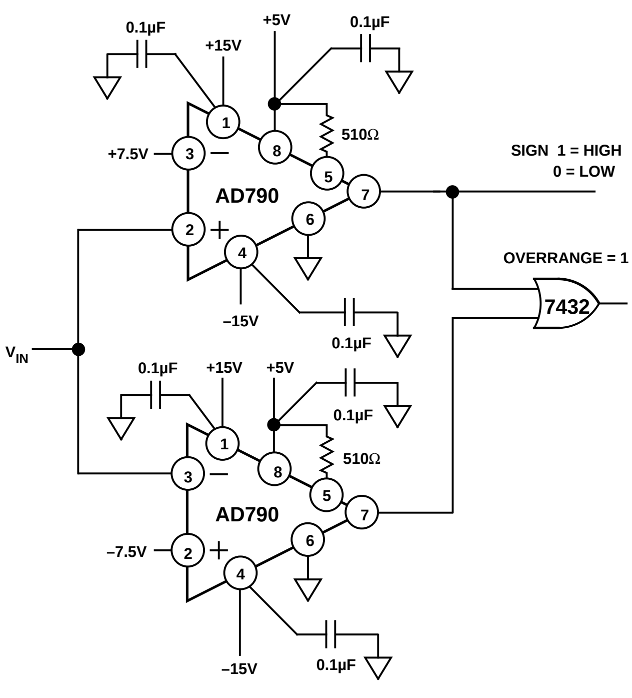


Figure 16. Overvoltage Detector (N, Q Package Pinout)

Single Supply Ground Referred Overload Detector

The AD790 is useful as an overload detector for sensitive loads that must be powered from a single supply. A simple ground referenced overload detector is shown in Figure 16. The comparator senses a voltage across a PC board trace and compares that to a reference (trip) voltage established by the comparator's minus supply current through a 2.7 Ω resistor. This sets up a 10 mV reference level that is compared to the sense voltage. The minus supply current is proportional to absolute temperature and compensates for the change in the sense resistance with temperature. The width and length of the PC board trace determine the resistance of the trace and consequently the trip current level.

$I_{LIMIT} = 10\ mV/R_{SENSE}$

R_{SENSE} = rho (trace length/trace width)

rho = resistance of a unit square of trace

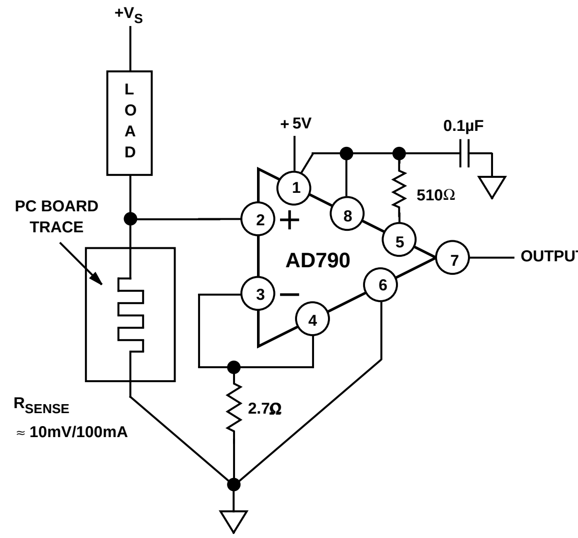


Figure 17. Ground Referred Overload Detector Circuit (N, Q Package Pinout)

Precision Full-Wave Rectifier

The high speed and precision of the AD790 make it suitable for use in the wide dynamic range full-wave rectifier shown in Figure 18. This circuit is capable of rectifying low level signals as small as a few mV or as high as 10 V. Input resolution, propagation delay and op amp settling will ultimately limit the maximum input frequency for a given accuracy level. Total comparator plus switch delay is approximately 100 ns, which limits the maximum input frequency to 1 MHz for clean rectification.

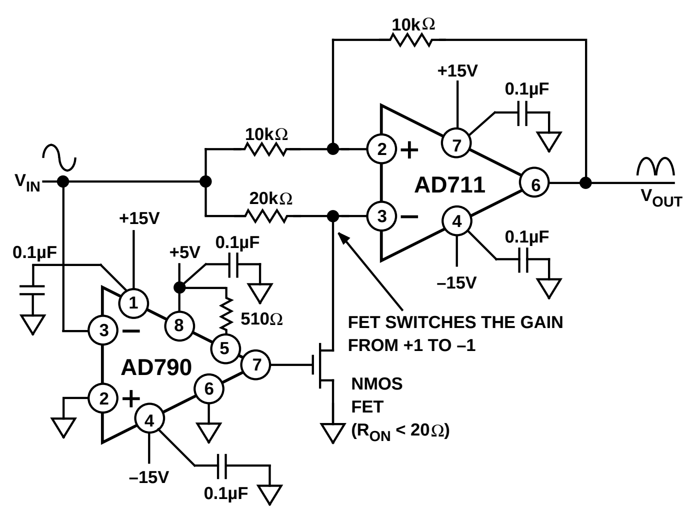
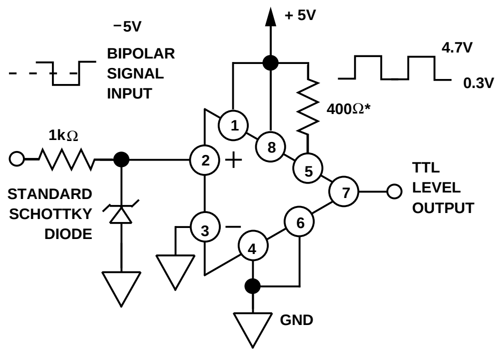


Figure 18. Precision Full-Wave Rectifier (N, Q Package Pinout)



*A RESISTOR UP TO 10kΩ MAYBE USED TO REDUCE THE SOURCE AND SINK CURRENT OF THE DRIVER. HOWEVER, THIS WILL SLIGHTLY LOWER THE MAXIMUM USABLE CLOCK RATE.

Figure 19. A Bipolar to CMOS TTL Line Receiver (N, Q Package Pinout)

Bipolar to CMOS/TTL

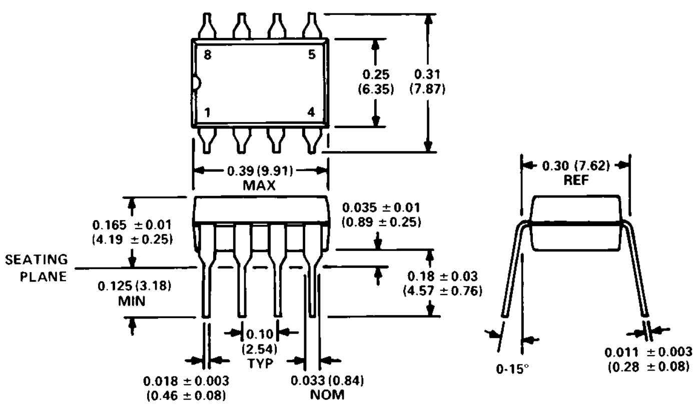
It is sometimes desirable to translate a bipolar signal (e.g., ±5 V) coming from a communications cable or another section of the system to CMOS/TTL logic levels; such an application is referred to as a line receiver. Previously, the interface to the bipolar signal required either a dual (±) power supply or a reference voltage level about which the line receiver would switch. The AD790 may be used in a simple circuit to provide a unique capability: the ability to receive a bipolar signal while powered from a single +5 V supply. Other comparators cannot perform this task. Figure 19 shows a 1 kΩ resistor in series with the input signal which is then clamped by a Schottky diode, holding the input of the comparator at 0.4 V below ground. Although the comparator is specified for a common mode range down to $-V_S$, (in this case ground) it is permissible to bring one of the inputs a few hundred mV below ground. The comparator switches around this level and produces a CMOS/TTL compatible swing. The circuit will operate to switching frequencies of 20 MHz.

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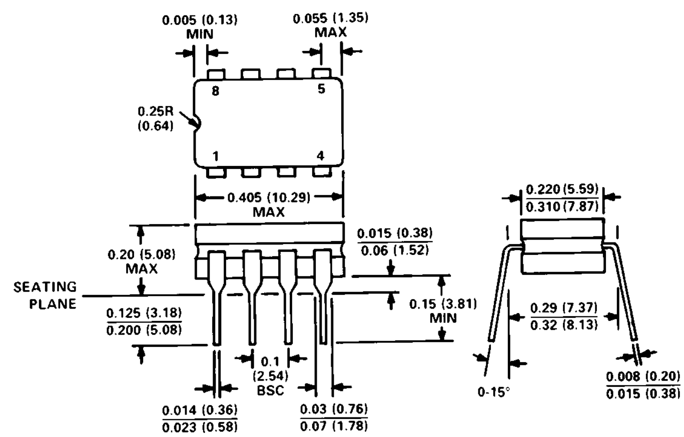
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

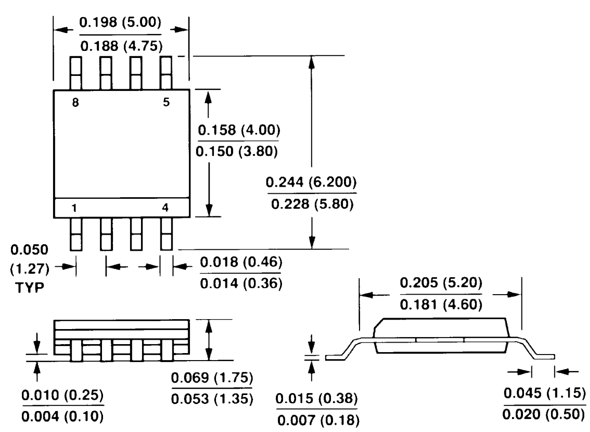
8-Pin Plastic Mini-DIP (N-8) Package



8-Pin Cerdip (Q-8) Package



SOIC (SO-8) Package



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